National Aeronautics and Space Administration

FPGA NEPP
FY08 Summary Report

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1 Overview

This report documents the activities and results of the Fiscal Year 2008 (FY08) funding for the NASA Electronic Parts and Packaging (NEPP) program for Re-programmable Field Programmable Gate Arrays (FPGA).

The FY08 task was divided into two sections. The first was focused on establishing a plan to develop long-term life-test reliability circuit designs with Xilinx, the manufacturer of the FPGAs of interest. Long-term life tests are the basic tool of technology analysis. Results from life tests are used to identify failure mechanisms and to provide quantitative estimates of device performance over the various required mission lifetimes.

The second section was to develop parametric test capability for state-of-the-art FPGAs. This test capability was developed with Integra Corporation. Parametric testing is the first line of electrical testing of FPGAs. Results from parametric testing are used to determine whether or not the device meets the manufacturer's data sheet specifications. Parametric testing is also used to determine quality and variability of devices obtained by a customer.

FPGA reliability analysis can be divided into two general areas, functional and parametric. Functional analysis is based on using high-level circuit designs made of combinatorial and sequential logic. Such designs will consume a wide variety of FPGA resources (i.e., LUT, RAM, Interconnect, etc.). Resource consumption will relate directly to power usage. Modern FPGAs are made with highly scaled complementary metal-oxide

semiconductor (CMOS) processes (130 nm and below). Such processes have significant performance and reliability concerns regarding static and dynamic power dissipation. Understanding power usage is a central requirement to understanding long-term FPGA reliability performance.

Parametric analysis of FPGAs focuses on the various currents and timings of the unprogrammed FPGA. Of particular interest is the behavior of these parameters as a function of temperature. Changes in current and timing as a result of changing temperature can often be related directly back to a fundamental physical process. This bifurcation of reliability analysis for this FY08 NEPP report is shown in Figure 1.

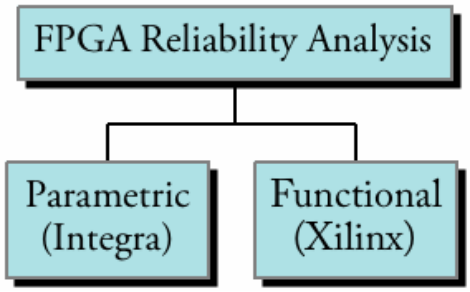

Figure 1. Overview implementation of FY08 NEPP FPGA task

2 Functional Reliability Analysis—Xilinx

Xilnx has developed a sophisticated reliability methodology to ensure high reliability for the FPGAs it produces. The methodology can be broken into four segments:

1. Design for Reliability
2. Technology Verification
3. Product Qualification
4. Continuous Monitoring and Feedback

Each segment is designed to address a different aspect of the overall FPGA reliability process.

The Design for Reliability segment is a rigorous model-based approach where circuit designs are made with models that already include wear-out effects. The Technology Verification step uses transistors and other custom test structures and vehicles. These structures are specifically designed to give insight into failure modes and to provide parameters that can be extracted for modeling support required in the Design for Reliability segment. These segments address intrinsic reliability problems such as electromigration and time-dependent dielectric breakdown.

The Product Qualification segment uses completed packaged parts that are fully tested and then subjected to a wide variety of environmental tests and stresses. Die and package interactions are also tested and evaluated at this phase. Finally, Xilinx maintains a Continuous Monitoring and Feedback process. This process of monitoring yields, defects, and many other manufacturing parameters in a rigorous and precise Statistical Process

Control (SPC) manner allows Xilinx to continuously identify and help eliminate any extrinsic problems that might affect overall reliability. This process is shown in Figure 2 [Pai 08].

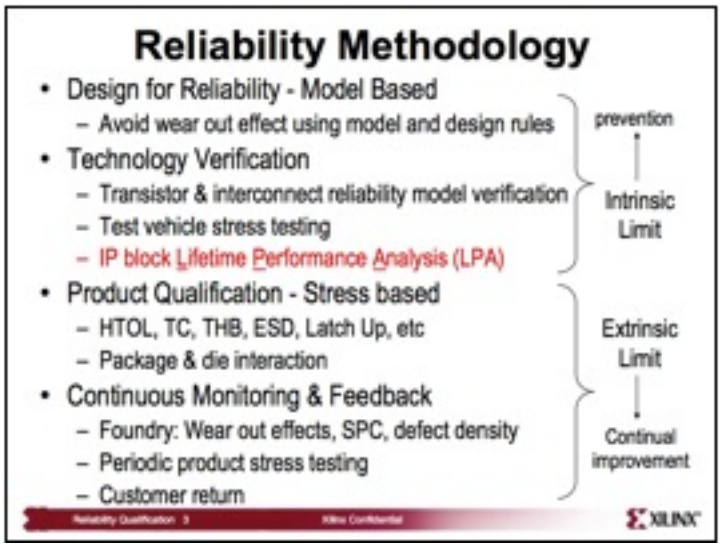

Figure 2. Xilinx reliability methodology

As semiconductor technology nodes continue to shrink, a wide variety of failure mechanisms have to be measured and understood. These include negative bias temperature instability (NBTI), hot carrier injection (HCI), electromigration (EM), and time-dependent dielectric breakdown (TDDB).

NBTI is of immediate concern in p-channel MOS devices stressed with negative gate voltages. NBTI manifests as an increase in the threshold voltage and a consequent decrease in drain current and transconductance. The degradation exhibits power law dependence with time [Peters 04]. HCI refers to either holes or electrons (also referred to as ‘hot electrons’) that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor (especially

MOS) device. Because of their high kinetic energy, hot carriers can get injected and trapped in areas of the device where they were not intended to be. This charge results in the formation of a space charge that causes the device to degrade or become unstable [Balkan 98].

Often simple transistors are used to test and characterize degradation effects like NBTI and HCI. A gradual shift of threshold voltage over time is commonly observed in p-type metal-oxide-semiconductor field-effect transistors (p-MOSFET or PMOS). This shift is caused by voltage stress on the gate oxide, temperature, and duty cycle of the stressing voltage (static stress as compared to dynamic stress). NBTI effects can limit the useful lifetime of CMOS devices.

To ensure a reliable design for possible NBTI effects, the bias conditions of each PMOS transistor must be considered. This consideration extends from the beginning of operational life throughout the expected lifetime of the product [Symko 07]. Typically, these conditions must allow for at least 10 years of operation at the highest voltage and the highest temperature. Static voltage stress shifts the voltage threshold roughly 10 times more than does dynamic stress. For example, a shift of 10 mV can occur in a dynamic (switching) situation, and a shift of 100 mV can occur in the static case [Chen 02].

To perform an NBTI study of a PMOS transistor, a constant negative bias is applied to the gate electrode at high temperatures with source, drain, and substrate grounded. The gate bias of a PMOS in a CMOS inverter is either at a high or low voltage, while the

drain bias is either low or high. It is important to investigate NBTI under such static (stuck at 1 or 0), as well as dynamic stress conditions. What is now required is to do a NBTI study on a test vehicle that is at a higher level of logical synthesis than a simple PMOS transistor. To accomplish this requires an examination of the logical building blocks available to the Xilinx FPGA user. Xilinx provides eight high-level Intellectual Property (IP) blocks on the Virtex 4. These IP blocks are the BRAM, DSP, DCM, FIFO, PLL, GCLK, RCLK, and IOCLK. Xilinx has begun to include use of these IP blocks as part of their reliability qualification [Lesea 05].

The Virtex 4 has up to 20 fully dedicated on-chip digital clock management (DCM) circuit blocks. The Virtex 4 DCM is a high-frequency digital circuit, designed to achieve picosecond precision and to provide a wide range of advanced clock management features. Each DCM contains more than a dozen finely tuned, multi-tap delay lines. These DCM circuit blocks are used to address on-chip clock distribution. Clock skew and clock delay will significantly impact device performance. Managing clock skews and delays with conventional clock trees becomes more difficult in larger FPGA devices like the Virtex 4. DCM circuits provide zero propagation delay and, along with fully differential global clock trees, low clock skew between output clock signals distributed throughout the device.

Xilinx's accelerated stress qualification testing showed that the DCM maximum operating frequency decreases if the DCM is held in a persistent static (non-operational) condition for an extended time. This means that the DCM might not achieve lock up to

the maximum frequency specifications. Static NBTI stress creates small variations in the duty cycle precision of each delay tap. Cumulatively, this variation reduces the maximum frequency at which the DCM can operate. Dynamic NBTI stress, however, does not lead to any reduction in performance because any voltage shift is applied equally to both of the matched PMOS transistors in each delay tap. Therefore, full performance is maintained if the DCM is placed into a continuous calibration mode (effectively toggling all delay taps) during periods of non-operation.

This is an important result. This documents a 'user' level functional block showing sensitivity and degradation directly relatable to a basic-device physics phenomenon. The levels of abstraction that the FPGA user community works in are many orders of magnitude above the basic technology level. Xilinx provided a range of solutions for Virtex 4 users to address this NBTI effect with the DCM.

These solutions avoid static NBTI stress either directly or by placing the DCM into a continuous calibration mode during periods of non-operation:

1. Static device burn-in (where the device is powered but unconfigured) is not permitted. Dynamic device burn-in (where the device is both powered and configured) is permitted as long as the DCMs are properly operated per certain conditions.
2. If the device is powered but stays unconfigured for an extended time then a null design, provided by Xilinx, must be loaded. The null design configures the DCMs into continuous calibration mode.

3. If the DCM input clocks stop for an extended time or the DCM reset is held asserted for an extended time then a drop-in macro is available to support these longer time durations.
4. Unused DCMs in designs are automatically configured into continuous calibration mode by the ISE 7.1i SP4 software.

Xilinx addressed this DCM sensitivity to NBTI by eventually re-designing the Virtex 4. However, automatic corrections were still needed to be made by the development software.

Using NBTI sensitivity on the Virtex 4 DCM as precedence, part of this NEPP task was to lay the groundwork needed to do a similar reliability evaluation on another block of Xilinx Virtex 4 IP. Xilinx has only done this type of testing on IP blocks BRAM, DSP, and DCM.

The remaining Virtex 4 IP blocks (FIFO, PLL, GCLK, RCLK, and IOCLK) are candidates for such an undertaking. Several meetings were held at Xilinx and a plan was put in place to use Xilinx's Design Services organization. Due to funding reductions in FY08, JPL was unable to implement this plan. The goal is to start this work in FY09.

3 Parametric Reliability Analysis—Integra

Parametric analysis of FPGAs involves measuring data sheet parameters. These include a wide range of DC currents and voltages as well as a large number of timing-related measurements. All FPGAs are subjected to a large array of parametric tests by the vendor (i.e., Xilinx) before they are deemed satisfactory for shipment to customers. The results of these tests are usually not available to users. Manufacturers will publish max/min values for parametric tests in their data sheets, however.

Parametric measurements are of significant interest in reliability analysis because they can usually be related directly to a physical process/condition. Changes in parametric measurements as a result of exposure to long-term environmental conditions provide insight into the mechanism causing the degradation. For high reliability required of NASA missions, understanding changes in parametric values, even if the values are still meeting manufacturer's specification, help accurately predict end-of-life conditions and support overall risk management. Many of the parameters have a non-linear response to changes in temperatures, for example. Such non-linearities make accurate lifetime prediction complicated.

For this experiment, JPL partnered with Integra Technologies to provide the parametric measurements on FPGAs. Integra has been a semiconductor test house for more than 20 years. The Xilinx Virtex 4 FX20 device was used for the test. The Virtex 4 FX20 has one PowerPC processor block with 17,088 CLB flip flops and 19,244 logic slices. There are

320 I/Os on the FX20. It is packaged in a 672-pin FGG package. Measurements were made on a Sentry series tester. An example of this tester is shown in Figure 3.

Figure 3. Integra parametric tester example

The goal of the parametric testing was twofold:

1. Establish and understand the amount of variation across a given lot of commercial off-the-shelf (COTS) FPGAs.
2. Determine temperature performance of critical measurements and relate that to underlying device/technology.

The DC parametric data were taken on 20 samples of Virtex 4 FX20 all from lot 87048. The results of this testing are summarized in Tables 1 and 2. Table 1 is for samples 1–10 and Table 2 is for samples 11–20. The two groups of parts were tested on different days; therefore, the data files are provided separately for each day's testing.

Table 1. Parametric results from samples 1–10 (lot 87048 Virtex 4 SX20)

(-)55C	MIN	MAX	MEAN	STDEV	-3stdev	+3stdev
Vkh_Vkl/Vkl_t(V)	-0.379	-0.338	-0.363	0.006	-0.380	-0.345
IOZ_Test/IOZL_test(uA)	-0.172	0.103	0.030	0.044	-0.103	0.163
IOZ_Test/IOZH_test(uA)	0.002	0.350	0.107	0.074	-0.115	0.329
timing_test/buffio_pins(ns)	5.625	5.937	5.797	0.089	5.531	6.062
timing_test/muxout(ns	7.656	7.812	7.718	0.081	7.477	7.960
timing_test/clk_out(ns)	256.900	258.100	257.380	0.620	255.521	259.239
timing_test/clk_setup(ns)	248.800	248.800	248.800	0.000	248.800	248.800
vol_voh_test/vol1_test(mV)	196.000	316.300	214.994	9.756	185.726	244.263
vol_voh_test/vol2_test(mV)	198.400	230.200	213.920	5.804	196.507	231.334
vol_voh_test/vol3_test(mV)	198.500	228.900	212.584	7.415	190.338	234.830
vol_voh_test/vol4_test(mV)	201.300	232.500	214.584	5.520	198.025	231.143
vol_voh_test/vol5_test(mV)	200.100	224.300	213.075	4.947	198.235	227.916
vol_voh_test/voh_test(V)	2.049	2.167	2.152	0.007	2.132	2.172
Input_Leakage_Test/IIL_test(uA	-0.201	0.095	0.022	0.045	-0.112	0.156
Input_Leakage_Test/IIH_test(uA	0.000	0.357	0.125	0.079	-0.112	0.362
ICC_Test/ICCOQ(mA)	0.143	0.160	0.148	0.006	0.129	0.167
ICC_Test/ICCAUX(mA)	8.068	8.456	8.231	0.117	7.881	8.581
ICC_Test/ICCTQ(mA)	211.000	244.300	230.500	10.587	198.738	262.262

25C	MIN	MAX	MEAN	STDEV	-3stdev	+3stdev
Vkh_Vkl/Vkl_t(V)	-0.323	-0.261	-0.288	0.010	-0.317	-0.259
IOZ_Test/IOZL_test(uA)	-0.032	0.095	0.033	0.036	-0.076	0.142
IOZ_Test/IOZH_test(uA)	0.004	0.342	0.102	0.070	-0.109	0.313
timing_test/buffio_pins(ns)	6.094	6.250	6.203	0.075	5.977	6.429
timing_test/muxout(ns	7.969	8.437	8.390	0.148	7.946	8.834
timing_test/clk_out(ns)	258.100	258.700	258.220	0.253	257.461	258.979
timing_test/clk_setup(ns)	248.400	248.800	248.480	0.169	247.974	248.986
vol_voh_test/vol1_test(mV)	238.200	360.100	260.566	12.394	223.384	297.748
vol_voh_test/vol2_test(mV)	239.300	286.700	258.952	8.434	233.651	284.253
vol_voh_test/vol3_test(mV)	240.100	284.400	257.205	10.283	226.355	288.055
vol_voh_test/vol4_test(mV)	243.300	285.900	260.079	8.137	235.668	284.489
vol_voh_test/vol5_test(mV)	242.000	282.100	258.119	7.692	235.042	281.196
vol_voh_test/voh_test(V)	1.993	2.121	2.100	0.009	2.071	2.128
Input_Leakage_Test/IIL_test(uA	-0.025	0.093	0.028	0.034	-0.074	0.131
Input_Leakage_Test/IIH_test(uA	0.010	0.261	0.105	0.070	-0.105	0.314
ICC_Test/ICCOQ(mA)	0.149	0.216	0.169	0.019	0.113	0.226
ICC_Test/ICCAUX(mA)	7.390	7.669	7.498	0.086	7.241	7.754
ICC_Test/ICCTQ(mA)	129.800	173.000	146.690	15.825	99.216	194.164

125C	MIN	MAX	MEAN	STDEV	-3stdev	+3stdev
Vkh_Vkl/Vkl_t(V)	-0.270	-0.222	-0.237	0.007	-0.257	-0.217
IOZ_Test/IOZL_test(uA)	-0.254	0.002	-0.116	0.054	-0.279	0.047
IOZ_Test/IOZH_test(uA)	0.102	0.520	0.259	0.080	0.020	0.498
timing_test/buffio_pins(ns)	6.250	6.562	6.468	0.109	6.141	6.796
timing_test/muxout(ns	8.594	9.219	8.922	0.227	8.242	9.602
timing_test/clk_out(ns)	258.700	258.700	258.700	0.000	258.700	258.700
timing_test/clk_setup(ns)	248.400	248.400	248.400	0.000	248.400	248.400
vol_voh_test/vol1_test(mV)	281.600	391.400	306.960	11.704	271.849	342.070
vol_voh_test/vol2_test(mV)	283.300	333.000	305.478	9.766	276.178	334.777
vol_voh_test/vol3_test(mV)	283.500	329.000	303.563	11.848	268.020	339.105
vol_voh_test/vol4_test(mV)	288.300	336.600	307.063	8.895	280.379	333.748
vol_voh_test/vol5_test(mV)	286.400	325.500	304.895	8.321	279.932	329.858
vol_voh_test/voh_test(V)	1.975	2.081	2.058	0.009	2.031	2.084
Input_Leakage_Test/IIL_test(uA	-0.270	-0.026	-0.137	0.051	-0.289	0.015
Input_Leakage_Test/IIH_test(uA	0.129	0.480	0.284	0.079	0.047	0.521
ICC_Test/ICCOQ(mA)	0.446	0.618	0.529	0.064	0.335	0.722
ICC_Test/ICCAUX(mA)	8.077	8.934	8.548	0.303	7.638	9.457
ICC_Test/ICCTQ(mA)	226.700	326.600	262.580	33.522	162.013	363.147

Table 2. Parametric results for samples 11–20 (lot 87048 V4 SX20)

(-55C)	MIN	MAX	MEAN	STDEV	-3stdev	+3stdev	OO3s
Vkh_Vkl/Vkl_t(V)	-0.391	-0.332	-0.366	0.009	-0.391	-0.340	1
IOZ_Test/IOZL_test(uA)	-0.009	0.109	0.031	0.034	-0.072	0.134	0
IOZ_Test/IOZH_test(uA)	-0.002	0.371	0.094	0.073	-0.126	0.314	3
timing_test/buffio_pins(ns)	5.625	5.937	5.791	0.093	5.514	6.069	0
timing_test/muxout(ns)	7.656	7.812	7.687	0.065	7.493	7.881	0
timing_test/clk_out(ns)	256.900	258.100	257.140	0.497	255.649	258.631	0
timing_test/clk_setup(ns)	248.800	248.800	248.800	0.000	248.800	248.800	0
vol_voh_test/vol1_test(mV)	196.200	322.900	213.544	6.907	192.824	234.264	22
vol_voh_test/voh_test(V)	2.040	2.170	2.152	0.007	2.132	2.173	22
Input_Leakage_Test/IIL_test(u	-0.010	0.101	0.035	0.032	-0.062	0.132	0
Input_Leakage_Test/IIH_test(u	0.003	0.341	0.098	0.074	-0.124	0.320	1
ICC_Test/ICCOQ(mA)	0.135	0.144	0.138	0.002	0.131	0.146	0
ICC_Test/ICCAUX(mA)	8.048	8.287	8.208	0.060	8.030	8.387	0
ICC_Test/ICCTQ(mA)	218.500	252.800	235.333	11.185	201.777	268.889	0
25C	MIN	MAX	MEAN	STDEV	-3stdev	+3stdev	OO3s
Vkh_Vkl/Vkl_t(V)	-0.318	-0.265	-0.282	0.007	-0.303	-0.261	35
IOZ_Test/IOZL_test(uA)	-0.025	0.101	0.029	0.034	-0.073	0.130	0
IOZ_Test/IOZH_test(uA)	0.010	0.520	0.109	0.075	-0.116	0.335	5
timing_test/buffio_pins(ns)	6.094	6.250	6.177	0.081	5.936	6.419	0
timing_test/muxout(ns)	7.969	8.437	8.385	0.127	8.003	8.767	1
timing_test/clk_out(ns)	258.100	258.700	258.140	0.155	257.675	258.605	1
timing_test/clk_setup(ns)	248.400	248.400	248.400	0.000	248.400	248.400	0
vol_voh_test/vol1_test(mV)	234.900	347.400	260.904	8.669	234.897	286.911	13
vol_voh_test/voh_test(V)	2.008	2.124	2.098	0.008	2.074	2.122	16
Input_Leakage_Test/IIL_test(u	-0.019	0.092	0.032	0.032	-0.064	0.128	0
Input_Leakage_Test/IIH_test(u	0.008	0.389	0.110	0.075	-0.115	0.335	3
ICC_Test/ICCOQ(mA)	0.151	0.191	0.174	0.011	0.141	0.207	0
ICC_Test/ICCAUX(mA)	7.271	7.649	7.474	0.112	7.138	7.810	0
ICC_Test/ICCTQ(mA)	121.400	161.000	143.167	12.417	105.915	180.419	0
125C	MIN	MAX	MEAN	STDEV	-3stdev	+3stdev	OO3s
Vkh_Vkl/Vkl_t(V)	-0.270	-0.222	-0.237	0.007	-0.257	-0.217	31
IOZ_Test/IOZL_test(uA)	-0.254	0.002	-0.116	0.054	-0.279	0.047	0
IOZ_Test/IOZH_test(uA)	0.102	0.520	0.259	0.080	0.020	0.498	3
timing_test/buffio_pins(ns)	6.250	6.562	6.468	0.109	6.141	6.796	0
timing_test/muxout(ns)	8.594	9.219	8.922	0.227	8.242	9.602	0
timing_test/clk_out(ns)	258.700	258.700	258.700	0.000	258.700	258.700	0
timing_test/clk_setup(ns)	248.400	248.400	248.400	0.000	248.400	248.400	0
vol_voh_test/vol1_test(mV)	281.600	391.400	306.960	11.704	271.849	342.070	9
vol_voh_test/voh_test(V)	283.300	333.000	305.478	9.766	276.178	334.777	0
Input_Leakage_Test/IIL_test(u	-0.270	-0.026	-0.137	0.051	-0.289	0.015	0
Input_Leakage_Test/IIH_test(u	0.129	0.480	0.284	0.079	0.047	0.521	0
ICC_Test/ICCOQ(mA)	0.446	0.618	0.529	0.064	0.335	0.722	0
ICC_Test/ICCAUX(mA)	8.077	8.934	8.548	0.303	7.638	9.457	0
ICC_Test/ICCTQ(mA)	226.700	326.600	262.580	33.522	162.013	363.147	0

Tables 1 and 2 contain mean, standard deviation, max, min, and 3-sigma values for all the measurements made. IOZ/Vkh and Vol/Voh measurements have 320 data points per device. The rest of the measurements are only 1 per sample. Measurements were made at 125°C, 25°C, and -55°C.

For most of the parameters, the standard deviation is a small (<5%) percentage of the mean. This means that the amount of variation in the parameter is small. There are a few parameters that have standard deviations that are almost as large as their means, however. These parameters are IOZL and IOZH. A sample of the IOZ data at -55°C is shown in Figure 4.

The probability plot in Figure 4 highlights the fact that IOZ data have an almost equal mean and standard deviation. There appear to be two distinct distributions of data; one from 0 to 0.02 µA and then another from 0.05 to 0.10 µA. The IOs are programmable on the V4 and the IOZ measurement is made of six different IO formats. Figure 5 shows the IOZ data broken out by IO type and plotted as box plot data.

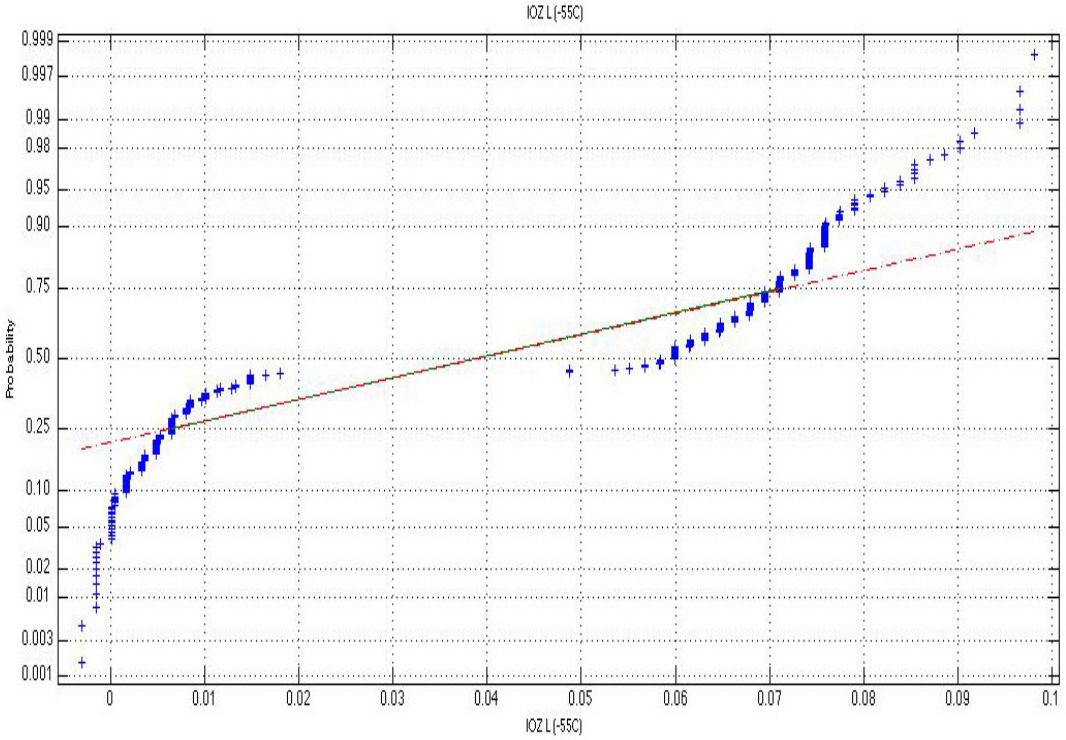

Figure 4. Probability plot of IOZ (-55°C) data

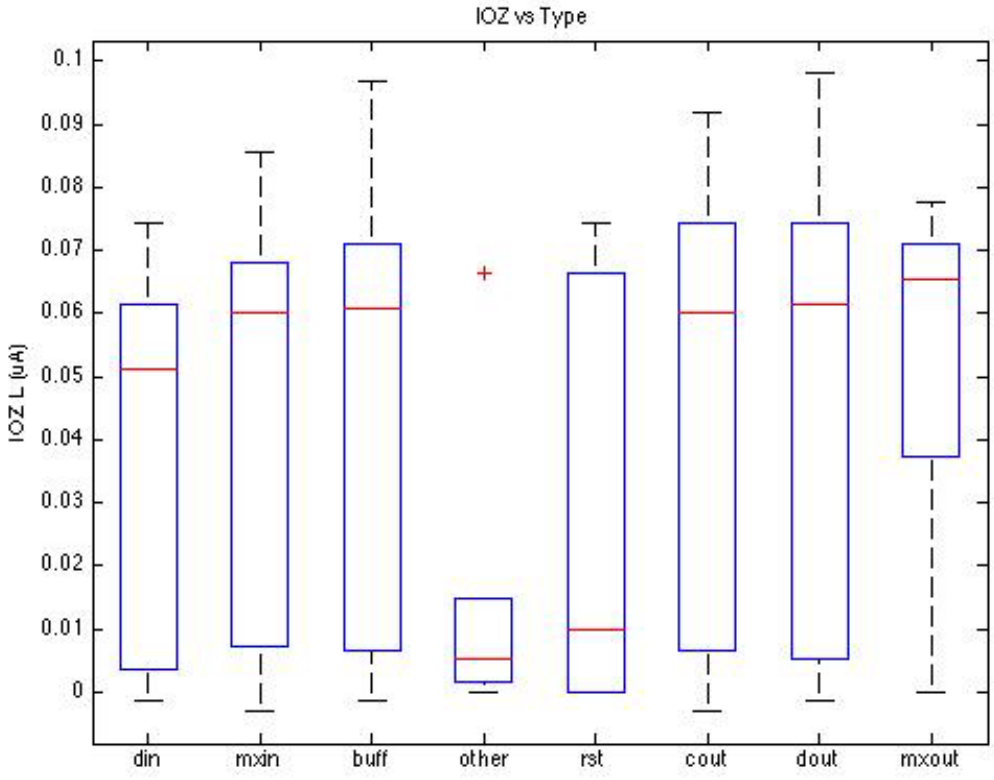

Figure 5. Box plot of IOZ data by IO

Figure 5 shows that all IOs have a similar degree of variation except for the "mxout" and "other." The "other" term is used to represent individual pins like LOAD, CE, SEL1, etc. The "mxout" pins have a similar mean but much smaller variation and spread. Figure 5 shows that the different IOs contribute equally to the variation in IOZ data.

Measuring current as a function of temperature is often one of the most critical parameters for determining overall technology capability as well as possible reliability concerns. There are three main currents that were measured on the V4 SX20s: core, IO, and auxiliary current. Figure 6 is a plot of the mean values for these three different current measurements as a function of temperature.

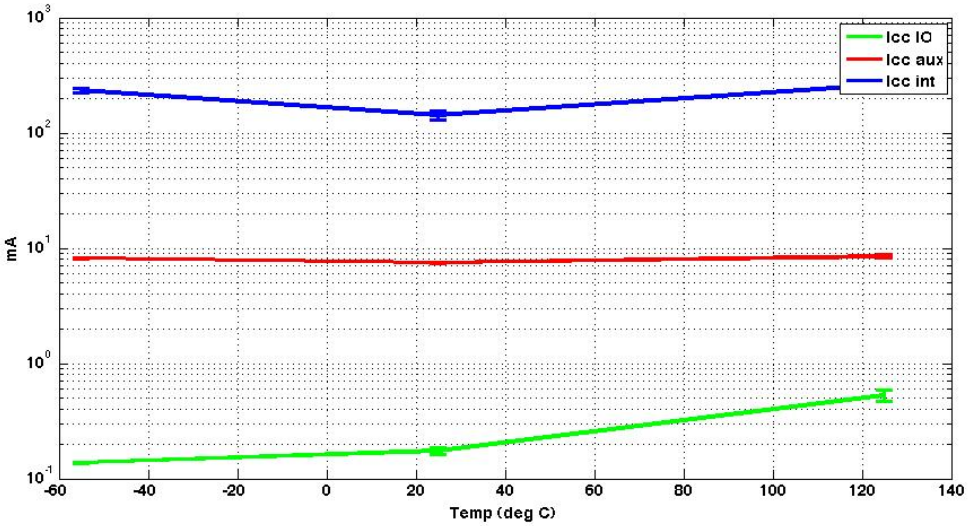

Figure 6. Current vs. temperature (blue = Int, red = Aux, green = IO)

There are two interesting effects in Figure 6. First, the IO current increases as a function of temperature from -55°C to 125°C. However, the core (INT) current has a minimum at 25°C while both the -55°C and 125°C values are higher. The increase of IO current as a function of temperature is expected due to the leakage currents associated with 90 nm CMOS. Such highly scaled CMOS has increased subthreshold leakage values. This subthreshold leakage is similar to diode/bipolar device leakage and is exponentially dependent on temperature.

Subthreshold leakage current (I_{sub}) is caused by minority carriers drifting across the channel from drain to source due to the presence of a weak inversion layer when the transistor is operating in cut-off region ($V_{GS} < V_{TH}$). The minority carrier concentration rises exponentially with gate voltage V_G, and so the plot of log (I_{sub}) versus V_G is a linear curve with typical slopes of 60–80 mV per decade. I_{sub} depends on the substrate doping concentration and halo implant, which modifies the threshold voltage V_{TH}.

$$I_{SUB} = I_O \left(1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right) \exp\left(q\frac{V_{GS} - V_{TH} - V_{OFF}}{nkT}\right)$$

where V_{OFF} is the offset voltage in sub-threshold region and I_O is given as:

$$I_O = \mu \frac{W_{eff}}{L_{eff}} \left(\frac{kT}{q}\right)^2 \sqrt{\frac{q\varepsilon_{si} NDEP}{2\phi_3}}$$

The result of a temperature minimum with the core (INT) current was not expected. As a result, additional analysis was performed on the INT data. This is shown in Figure 7. Figure 7 is a probability plot of the INT data for the three temperatures. Figure 7 shows that the three temperatures are each separate distributions. The -55°C and 25°C values have similar slopes. The -55°C distribution could be interpreted as the 25°C distribution with the addition of a 90 mA offset current. The 125°C has a reduced slope indicating a larger amount of variation in the data.

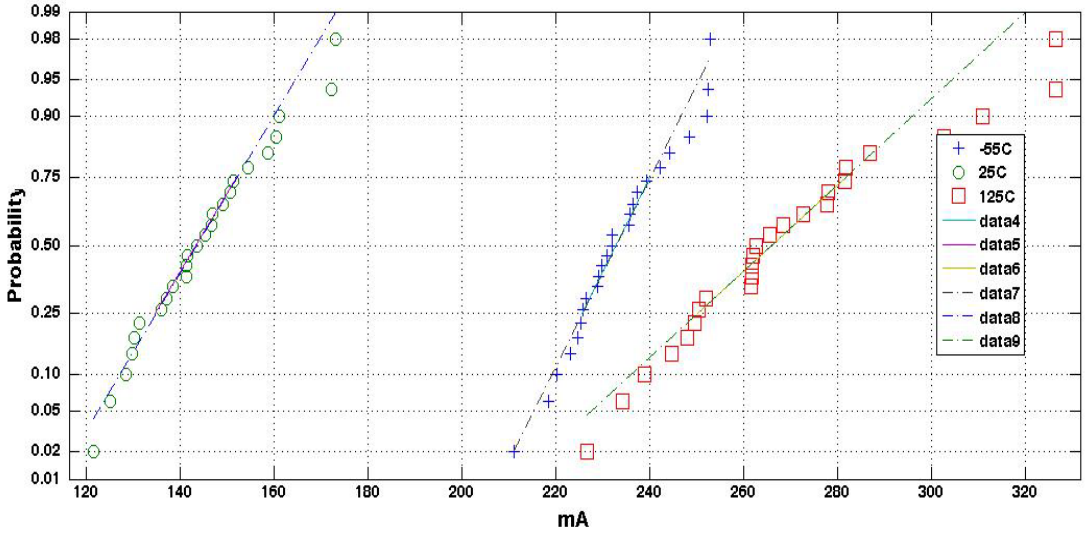

Figure 7. Probability plot of three temperature core (INT) current (ICCINTQ—Quiescent VCCINT Supply Current, V4 FX20, Lot 87048)

During factory characterization, Xilinx configures the FPGA with a propriety blank design. This blank design results in the part doing nothing; no output current loads; no active input pull-up resistors; and all I/O pins, 3-state and floating. Xilinx uses this design for their initial characterization process and does not share the blank configured design with third parties.

These measurements were taken using an Integra design. This results in the part being configured. This means there may be some dynamic element involved internally on the part; also, it may be related to configuration pull ups/downs and how the unused pins options are set. To test this, this ICCTQ static test was then performed on an unconfigured device. The results of this comparison test are shown in Table 1.

The current increases as the temperature increases for the unconfigured device. This is in contrast to the configured device that shows minimum values seen at 25°C and 70°C while the -55°C and 125°C values increase. Table 1 suggests that the ICCTQ minimum at the 25°C to 70°C range is due to the particular nature of the test design configuration implemented at Integra. The unconfigured design shows a quadratic increase in current as a function of temperature (R = 0.989).

Table 1. ICCTQ vs. configured and unconfigured

ICC_TQ (mA)				
Temperature	-55°C	25°C	70°C	125°C
Unconfigured	45.21	51.1	81.1	200.7
Configured	188.7	120.7	118.2	241.4

Xilinx FPGAs are known to have large start up currents at low temperatures [Burke 04]. They show a Virtex 1 requiring approximately 1.8 A of startup current at -55°C compared to 0.5 A of startup current at 25°C. SRAM-based FPGAs, like the Xilinx Virtex series, are known to have large startup (in rush) currents due to the large number of transistors that are at indeterminate states at time t = 0. SRAM-based FPGAs can also consume extra current during the configuration stage as a result of programming requirements.

MOSFET drain current varies considerably with temperature. The change in drain current can be over 20% for the -55°C to 125°C temperature range. NMOS devices have larger change than PMOS devices. The temperature coefficient of drain current can be positive, negative, or zero depending on operating voltage. This effect is shown in Figure 8 [Arora 06].

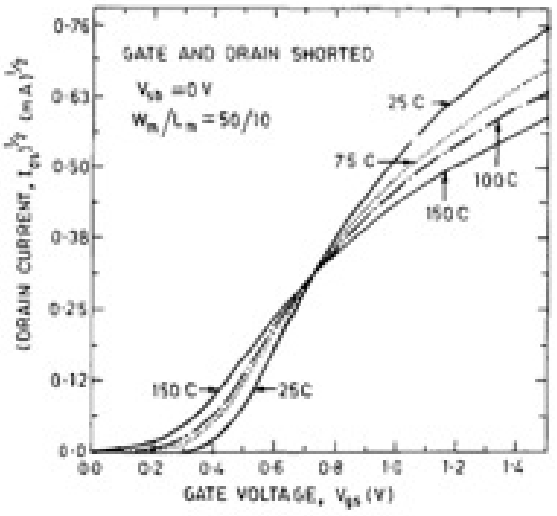

Figure 8. Transistor drain current (*Id*) vs. gate voltage (*Vgs*) vs. temperature

Carrier mobility, intrinsic carrier concentration, threshold voltage, and carrier saturation velocity are all functions of temperature, contributing to this operation dependence. Routing in FPGAs contributes more to higher leakage power than logic blocks. The reason for this is that the number of transistors in the routing fabric is much higher than in logic blocks. Logic elements consist of 4-input Look Up Tables (LUTs) and input multiplexers while connection blocks and switch blocks are made up of large numbers of buffers and pass transistors.

4 Conclusions

This report has detailed the FY08 NEPP FPGA program results. The FY08 program was focused on developing practical designs and testing schemes for the evaluation of long-term reliability issues related to the use of reprogrammable FPGAs. The sensitivity of basic Virtex 4 IP blocks to transistor degradation was shown. This validates this approach as a methodology for future screening and test proposals.

A parametric test capability was developed for Virtex 4 as well. The variation of commercial devices was shown to be well in control. This means that possible parametric measurement shifts would be an accurate indicator of degradation as a result of exposure to accelerated environments. A non-linear temperature dependence of certain FPGA design-specific currents has also been identified. This design dependence is an important result for space applications where wide temperature range performance may be required. Being able to accurately characterize each flight design is an important capability for overall risk mitigation for the use of FPGAs at NASA.

It is recommended that follow-on work take advantage of the capability developed by this task at Integra. Being able to measure parametric values before and after a particular environment stress would allow NASA to get a detailed understanding of possible shifts or degradations in Xilinx FPGA performance. Such shifts are usually the precursor to more catastrophic failures. A specific Virtex 4 SX20 based design could also be developed and tested parametrically before and after long-term stress, using a more generic reliability test or mission specific timeframe and conditions.

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